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Reduction of Processing Time to Improve Latency in Wireless Communication Network

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Abstract

The latency in Long Term Evolution (LTE) needs to be reduced to a desired low level to meet the expectation of 5G, which is the entry level for future wireless communication network. The latency is significantly affected by the delay in the data processing for both uplink and downlink. In this paper, reduction of processing time for data transmission has been proposed for delay consumption of wireless communication network.

Keywords: latency reduction; processing time; LTE

1. INTRODUCTION

In LTE, 14 orthogonal frequency division multiplexing (OFDM) symbols span a 1 ms duration, called subframe. The subframe is an actual and typical transmission time interval (TTI) of data. LTE uses data partitioned into transport blocks (TBs) and every TB is transmitted on a subframe, using a number of resource blocks (RBs). The standard constrains the use of only one modulation and coding scheme (MCS) for a TB, although the RBs can be located at different frequencies with various radio link qualities. As an attempt for reliable delivery of TBs, HARQ, a combination of Forward Error Correction (FEC) and ARQ, is used with a maximum of three retransmissions. For either a new transmission or a retransmission, the TB is generated after obtaining the information of the number of RBs and MCS, to be used. However, for the purpose of link adaptation and resource management, the eNodeB updates its decision for the number of RBs and MCS right before every TTI or subframe.
To improve latency in LTE, in previous the authors proposed a scheme with feedback, namely, early decoding, in which a single decoding is attempted at a time, determined based on the available channel state information. The authors showed that shorter TTI reduces latency. The latency reduction using slotted TTI is also shown. Some authors also suggested for reordering the IFFT input data to improve latency. Latency reduction in LTE using new technique named DASH MPD has been introduced. Two scheduling methods to reduce latency in LTE are also

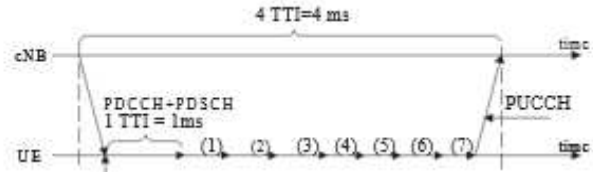
proposed earlier. Latency reduction techniques were studied for LTE in Rel. 14 and the outcome yielded a layer 2 solution in Rel. 14 and a layer 1 solution in Rel. 15. The layer 2 solution allowed the UE to skip uplink transmission if the UE has no data. Here a network can configure the uplink resources without data buffer of UE. The layer 1 solution includes two sub-solutions: 1. Shortened processing time for 1ms TTI 2.Shortened TTI with shortened processing time.

In this paper, short processing time n+2 is acquainted with improving latency. With TTI length not transformed, it is attractive to abbreviate the handling time of 1ms TTI particularly in the client equipment (UE) side, taking into account that the ability of the developed NodeB(eNB) will never be an issue.

The remainder of this paper is organized as follows. The proposed method to reduce latency is explained in Section 2. In Section 3, we develop a numerical analysis to estimate the improvement from the proposed method. Finally, the whole paper is concluded in Section 4.

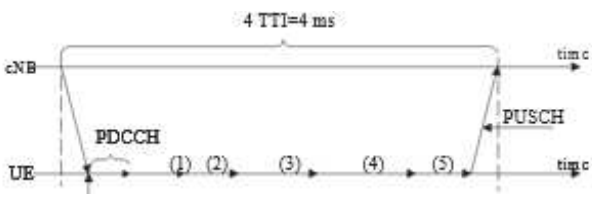
2. PROPOSED METHOD

Transmission of downlink (DL) or uplink (UL) information with HARQ requires an affirmation (ACK or Negative ACK) that sent the other way to demonstrate the achievement or failure of the bundle gathering. On account of recurrence division dual (FDD) activity, affirmation pointers identified with information transmission in a subframe n are transmitted the other way during subframe n+k, where the estimation of k is fixed to4 and the subframe length is equivalent to the TTI length. Preparing time and TTI lengths are the critical parameters of this interim. Contrasted and eNB, the handling time for the most part depends on UE ability. Accordingly, this paper centers around processing time between DL information and DL HARQ or between UL award and UL data. So as to reduce the delay time, different approaches can be considered to the few parts of the processing time of current activity. Fig 1 and fig 2 show the detailed proposed processing procedure.



(0) Start to receive DL TTI
(1) Do FFT
(2) Detect and decode DL assignment
(3) PDSCH channel estimation
(4) PDSCH data turbo decoding
(5) Create UL channel with HARQ-ACK
(6) Do IFFT
(7) Power control

Fig 1. Proposed processing procedure between DL data and DL HARQ



(0) Start to receive DL TTI
(1) Do FFT
(2) Detect and decode UL grant/PHICH
(3) PUSCH data turbo coding
(4) Do DFT and IFFT for PUSCH
(5) Power Control

Fig 2. Proposed processing procedure between UL grant and UL data.

2.1 Maximum TA

In the inheritance 1ms TTI activity without confinement of the maximum transport square size (TBS), the accessible processing time between DL information and DL HARQ or between UL award and UL information is 4ms-time advance (TA), where TA is double the size of the spread deferral among UE and eNB. The current heritage handling time of n+4 is set based on the most extreme TA of 0.67ms, comparing to 100km site radius. Plainly the greatest TA can be limited for processing time decrease. Take the most extreme site sweep of 25km as model, the greatest TA is diminished to 0.16ms,corresponding to a sparing of 0.51ms. The shorter the maximum TA, the bigger efficient can be accomplished. Consequently, restricting the most extreme TA would then help accomplish abbreviated timing for inheritance TTI.

2.2 Maximum TBS

Among the segments of the preparing time, some are the fixed time not identified with TBS, while the else can scale with some methodologies or confinements. A few stages that associated with the time-area asset length of PDCCH and/or physical downlink shared channel (PDSCH) locale can't be reduced. The progression of (0) in figure 1 is the fixed 1ms and the progression of (0) in figure 2 relies upon the time-space resource length of PDCCH locale. The quick Fourier change/inverse fast Fourier change (FFT/IFFT) activity is irrelvant with TBS, which are the fixed handling time, for example, the means of (1), (6) in figure 1 and the means of (1), the IFFT procedure of (4) in figure 2. The hour of these means can be composed as T fixed. A few stages are identified with the chip handling speed. The steps of (2), (5), (7) in figure 1 and the means of (2), (5) in figure 2 can directly scale with the expansion of chip preparing speed, the time of these means can be composed as Tchip. The other steps are identified with TBS, for example, the means of (3), (4) in figure 2 and the steps of (3), the discrete Fourier change (DFT) procedure of (4) in figure 2. Confinement can be set on the TBS to reduce processing time of PDSCH/PUSCH coding. However, TBS is reliant upon tweak and coding plan (MCS)and the quantity of asset squares (RBs) doled out to UEs. The heavier TBS limitation would influence the range efficiency and result into lower cell throughput. In this way, the degree of TBS confinement ought to be considered.

3. NUMERICAL ANALYSIS

Processing time between DL data and DL HARQ can be written as

$$m\,(4\ -\ 0.67\ -\ 1 - T_{chip} - T_{fixed}) + T_a + 1 + T_{chip} + T_{fixed} \tag{1}$$

where m is the maximum TBS reduction factor ($0 < m < 1$),and T_a is the current TA assumed to be reduced to 0.33ms,considering that the site radius for 1ms TTI should not be too small. If assumed that a processing time of n+2 wants to be achieved, then the formula (1) can be expressed as

$$m(4\ -\ 0.67 - 1 - T_{chip} - T_{fixed}) + T_a + 1 + T_{chip} + T_{fixed} < 2$$

$$m\,(1.83) + 0.16 + 1 + 0.5 < 2$$

$$m\,(1.83) < 2 - 1.66 \tag{2}$$

and$m$can be further expressed as

$$m < 1 - [0.66 / \{\ 1.30 - (T_{chip} + T_{fixed})\ \}] \tag{3}$$

The time of turbo coding/decoding occupies a large proportion in the processing time and if assumed that $T_{chip} + T_{fixed} = 0.50$ms, m would be equal to 0.18.

Take time-domain resources into account, it is desirable to assume that the maximum supported TBS is at most restricted to one seventh, compared with the TTI length of two OFDM symbols. Thus, the parameter m can be a reasonable TBS restriction.

Similarly, the needed processing time between UL grantand UL data can be written as
$m\,(4\ -\ T_{PDCCH} - 0.67\ -\ 1 -\ T_{chip} - T_{fixed}) + T_a + 1 + T_{chip} + T_{fixed} + T_{PDCCH}$

$$m\,(4\ -\ 1.19 - 0.67\ -\ 1 -\ T_{chip} - T_{fixed}) + 0.16 + 1 + T_{chip} + T_{fixed} + 1.19 \quad (4)$$

where T_{PDCCH} is the length of PDCCH region and if assumed that the PDCCH region occupies 2 symbols, m can be further expressed as

$$m < 1 - [0.66 / \{\ 2.70 - (T_{chip} + T_{fixed})\ \}]$$

where the possible m is equal to 0.70

So in both cases DL and UL, the value of m has been satisfied by the condition ($0 < m < 1$)

As talked about above, there are sufficient proof to help that it is conceivable to accomplish to accomplish a n+2 handling timing with the limitation of both greatest TA and most extreme TBS. Considering that there are some extra approaches to achieve more idleness decrease, for example, quicker chip preparing speed, itis attractive to recommend that with short preparing time of 0.50ms TTI, a n+2 processing time can be supported.

4. CONCLUSION

In this paper, we present short processing time to fulfill the requirements on low latency. Short processing time can be obtained with restriction on the maximum TA and TBS. The maximum TA is related to the site radius and current TA is assumed to be reduced to 0.16ms, resulting into a saving of 0.51ms. The maximum TBS restricted to one half is enough to support a n+2 processing timing along with TA reduction. It is obvious that just using short processing time can bring a support of n+2 processing timing.

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